

**AN INVESTIGATIVE REDESIGN OF THE ECG AND EMG SIGNAL CONDITIONING
CIRCUITS FOR TWO-FAULT TOLERANCE AND CIRCUIT IMPROVEMENT**

Final Report

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INTRODUCTION

An investigation was undertaken to make the electrocardiography (ECG) and the electromyography (EMG) signal conditioning circuits two-fault tolerant and to update the circuitry. The present signal conditioning circuits provide at least one level of subject protection against electrical shock hazard but at a level of 100 μA (for voltages of up to 200 V). However, it is necessary to provide catastrophic fault tolerance protection for the astronauts and to provide protection at a current level of less than 100 μA . For this study, protection at the 10 μA level was sought. This is the generally accepted value below which no possibility of microshock exists. Only the possibility of macroshock exists in the case of the signal conditioners. However, this extra amount of protection is desirable. The initial part of this report deals with current limiter circuits followed by an investigation into the signal conditioner specifications and circuit design.

CURRENT LIMITERS

JFET Limiters

There are several ways to limit the amount of current that flows into a subject that is connected to an instrument via electrodes. The choice of method depends on the origin of the current. The current may come from the instrument's own power supplies or from an external source returning to that source's ground via the instrument.

One protection technique is to insure that there is no connection between the instrument and the external source's ground. This can be done using isolation techniques such as infrared or transformer coupling. This technique was rejected in the case of the signal conditioners for two reasons. First, the isolation devices consume large amounts of power (supply currents in the 4 to 10 mA range) and second, they will not protect against the dc current that could flow into the subject from the power supply on the subject side of the isolation system.

Another type of current limiter is the input to the instrumentation amplifier that will be used in the signal conditioners. Under normal circumstances very little current flows into this terminal. The current that does flow is the bias current for the operational amplifiers (op amps) of the instrumentation amplifier. These currents can be as low as 6 nA for some BJT op amps or as low as the 30 pA for FET op amps. However, these are the currents that flow when the op amps are in their nonsaturated mode of operation. Little is known about how much current would flow if the op amp should saturate or if excessive input voltage should cause a break down of the op amp input stages. For these reasons it is not reasonable to count the input stages of the instrumentation amplifier as a current limiter.

Current limiters can be made from semiconductors. Most circuits use JFET circuits since they are depletion devices and lend themselves to passive operation. However, current limiters can be also made from diodes. The various types of circuit designs have their own advantages and disadvantages. Several designs will be

presented and discussed.

Figure 1 shows the current limiter that is used in the present signal conditioning circuits. It is composed of two n-channel JFETs and three resistors. For low current flowing through the device from the left to the right, Q1 and Q2 initially have low resistance which is much lower than R1. As the current increases, the voltage across R1 increases to the pinch off, V_p , value of Q1. Then Q1 limits the current through the device to a value of approximately $V_p/R1$. Q2 remains as a low resistance. The role of Q1 and Q2 reverse as the current through the device reverses. R2 and R3 are necessary if V_p is larger than .7 V (the turn-on voltage of the diode formed by the gate and channel). Regardless of the value of V_p , including these resistors is a good idea and their value should be fairly large. Figure 2 shows the current through the device as predicted by SPICE. For this run the FETs had a pinch-off of .5 V and an I_{DSS} of 4 mA. (As long as I_{DSS} is of a normal value, i.e., the mA level, this parameter has no effect on the maximum current limit value for this and the other circuits to be discussed.) The resistor R1 was 50 k Ω and R2 and R3 were 1 M Ω . The

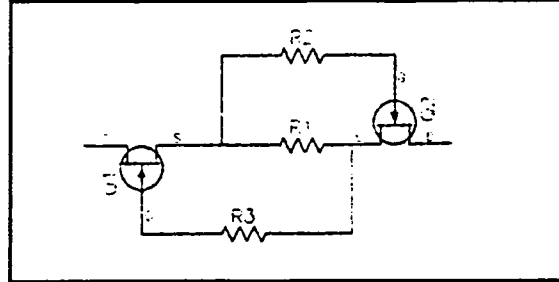


Figure 1. Simple JFET Current Limiter.

advantages of this circuit are that there are few parts and only n-channel FETs are required. The dynamic "on" resistance of this circuit is approximately R1 which is 50 k Ω in the above example. The disadvantage of this circuit and all JFET circuits is that the pinch-off voltage must be small to keep the size of the resistor R1 small for a given maximum current flow. Also the breakdown voltage for each device must be larger than the maximum voltage that the subject could ever encounter. JFETs that have low pinch-off voltage and high breakdown voltage are difficult to obtain.

Another type of current limiter circuit is shown in Figure 3. This device has four JFETs, two n-channel and two p-channel. The bidirectional current through this

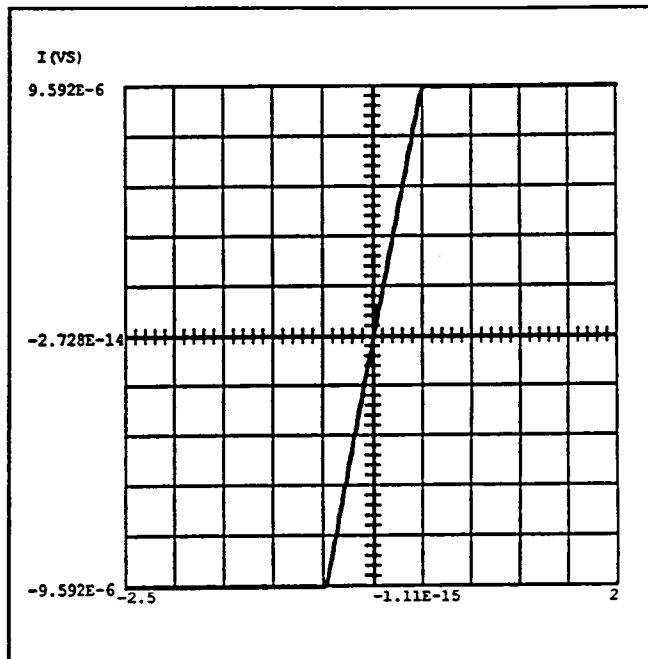


Figure 2. Current through the Limiter of Figure 1.

device is shown in Figure 4 which was generated with SPICE. The pinch-off voltages for these FETs were .5 V. To obtain a maximum current flow of FETs approximately 10

μA , R_1 and R_4 were 50 k Ω . The other resistors were large at 1 M Ω . The "on" resistance of this device is R_1 plus R_4 . The maximum current flow is $V_p/(R_1+R_2)$. An advantage of this circuit is that after the voltage across the device gets to $2V_p$ the current flow is reduced to approximately zero. An other advantage is that for given device breakdown voltage the voltage is divided between one of the n-channel and p-channel FETs. Thus, if the overall device breakdown voltage needs to be 200 V, each FET only needs to withstand 100 V. One of the disadvantages of this circuit is the large "on" resistance. It is twice that of the circuit of Figure 1 for the same pinch-off voltages and maximum current.

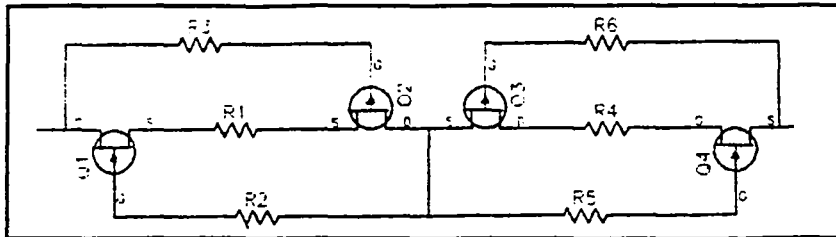


Figure 3. Limiter Using Both n- and p-channel FETs

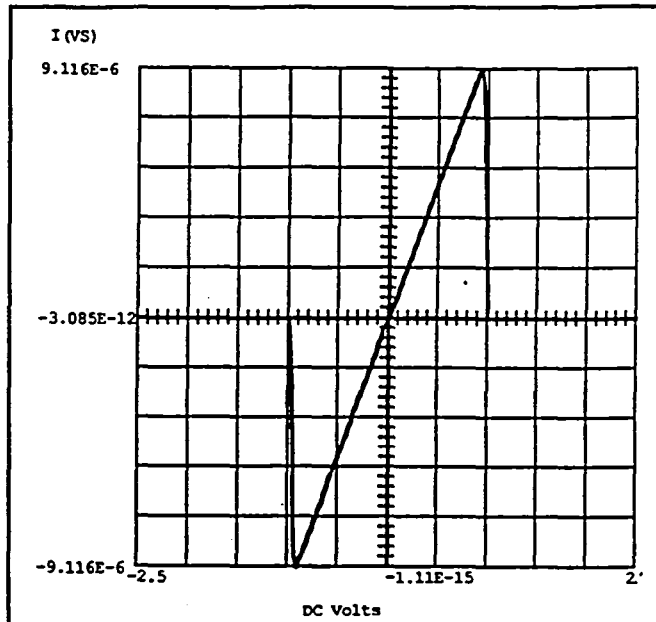


Figure 4. Current Through the Limiter of Figure 3.

The final JFET circuit to be presented is a slightly modified version of the patented circuit used in the Cherne Medical current limiter (Kroll, 1988). The circuit is shown in Figure 5. It is composed of 6 JFETs (4 n-channel and 2 p-channel) and several resistors. This circuit is similar in response to the circuit of Figure 3. That is the current reaches a peak value of approximately V_p/R_2 as the voltage across the device increase to V_p and declines to a minimum when the voltage reaches $2V_p$. The value of this minimum (left-to-right) current is $(V_p - .5 \text{ V})/R_3 + (V_p - .5 \text{ V})/R_5$. The .5 V is that voltage at which the diodes formed by Q3 and Q6 just start to turn on. The "on" resistance of the device is approximately R_2 . Figure 6 shows the SPICE predicted current for the device with all FETs having $V_p = .5 \text{ V}$, $R_2 = 50 \text{ k}\Omega$, and the other resistors equal to . 1 M Ω . If all resistors but R_2 are increased to 1 M Ω the current when the device is hard limiting is approximately .2 μA . The only advantage of this circuit over the circuit of Figure 4 is that, for the same current limit and V_p of the FETs, the "on" resistance is half as much. As with

the circuit of Figure 4, considering only left to right current flow, the breakdown voltages of Q1 and Q4 need only be one half that required for the complete limiter. The disadvantage of this circuit is its large parts count and the fact that it requires both n-channel and p-channel FETs.

The above circuits were fabricated, except with devices with V_p 's greater than .5 V, and their general characteristics verified. In all cases, when the devices were on and not limiting, they behaved like pure resistors.

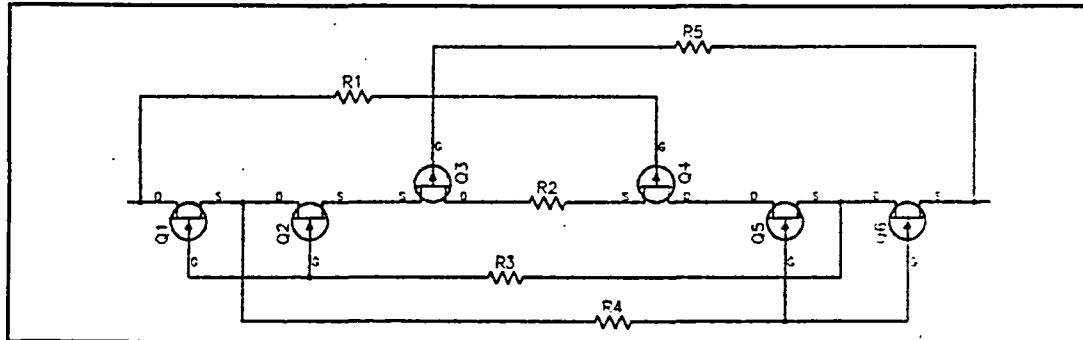


Figure 5. Modified Cherne Current Limiter.

It should be pointed out that actual testing of the Cherne Medical current limiter shows it to follow the SPICE predicted current vs voltage curve except in the hard limit region. In this region the predicted current is .56 μ A while the actual testing plus the published advertised value is about 5 μ A. The reason for this discrepancy is not clear.

Diode Limiters

As mentioned earlier, current limiters can be made from diodes. The ideal diode equation is given as follows

$$i_d = I_s (e^{v_d/nV_T} - 1) . \quad (1)$$

Where I_s is the reverse saturation current, n is a constant that is approximately 1 for germanium diodes and 2 for silicon diodes, and V_T is a constant equal to about 25 mV at room temperature. When the diode is reverse biased, the current is constant at a value of I_s . If the reverse saturation current had a value of 10 μ A and two of these diodes were placed back-to-back as shown in Figure 7, then an ideal current limiting device would be obtained. The "on" conductance of the one diode can be found by differentiating equation (1) above with respect to v_d . The result when inverted gives the "on" resistance of one diode as

$$R_{on} = nV_T / I_s . \quad (2)$$

For $n = 2$ and $I_s = 10 \mu$ A the "on" resistance for a single diode would be 5 k Ω and 10 k Ω for the pair. The breakdown voltage of each would have to be in excess of that

required for the current limiter (200 V for this design).

Unfortunately, the diode current in the reverse direction is not constant. It continues to increase slowly until the breakdown region, with its characteristic knee region, is reached. Designing a current limiter using diodes made from silicon is not practical since the devices have I_s values in the nA range. This makes the "on" resistance unacceptably large from the stand point of thermal noise voltage plus if BJT op amps are used it is difficult to get the required bias currents through the limiter. Germanium diodes have reverse saturation currents about a thousand or more times larger than silicon diodes and they typically have low breakdown voltages.

A diode that can be used as a current limiter is the 1N277J. This device is supplied by BKC International¹. This is a germanium diode that has a breakdown voltage of about 125 V. Because of this relatively low breakdown voltage two of the diodes were placed in series and the voltage vs current curve in the reverse biased region generated. This graph is shown in Figure 8. As can be seen from this figure the current through the series pair is less than 10 μA for voltages below -255 V. This is the corner of the knee region because at a voltage of -280 V the current increases to almost 100 μA . Curves for several pairs of diodes were generated with approximately the same results. As can be seen from the steepness of the curve near the origin, the "on" resistance of the series pair is very high. The measured value is about 105 k Ω . For two pair of diodes placed back-to-back to obtain current limiting in both directions, the "on" resistance is about 210 k Ω . To reduce this resistance three of these limiters could be placed in parallel. The "on" resistance will drop to about 70 k Ω and the total current through the device at 200 V would only be about 20 μA . Twelve diodes would thus be needed for the construction of one limiter device. These diodes are not available in die form. Therefore, with the standard DO7 package, a large amount of

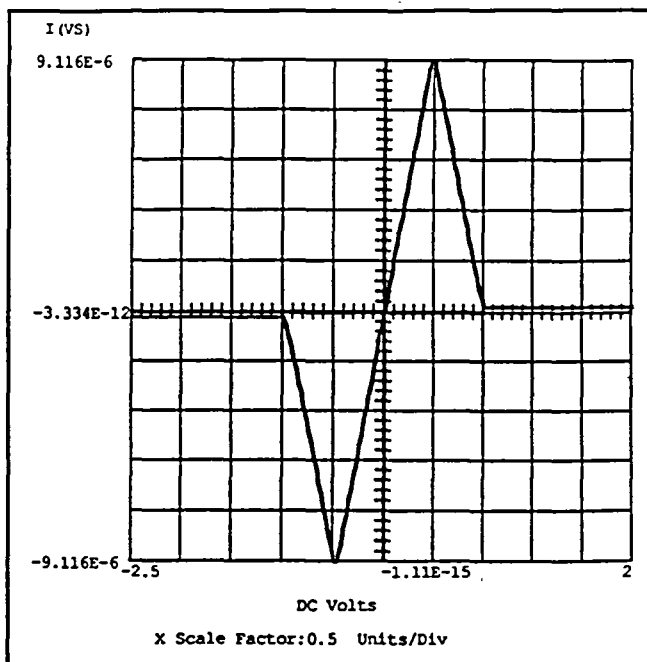


Figure 6. Current Through the Limiter of Figure 5.

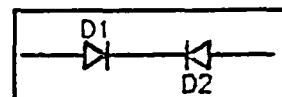


Figure 7. Diode Current Limiter.

¹BKC International Electronics, Inc., 6 Lake Street, Lawrence, MA 01841, (508) 681-0392

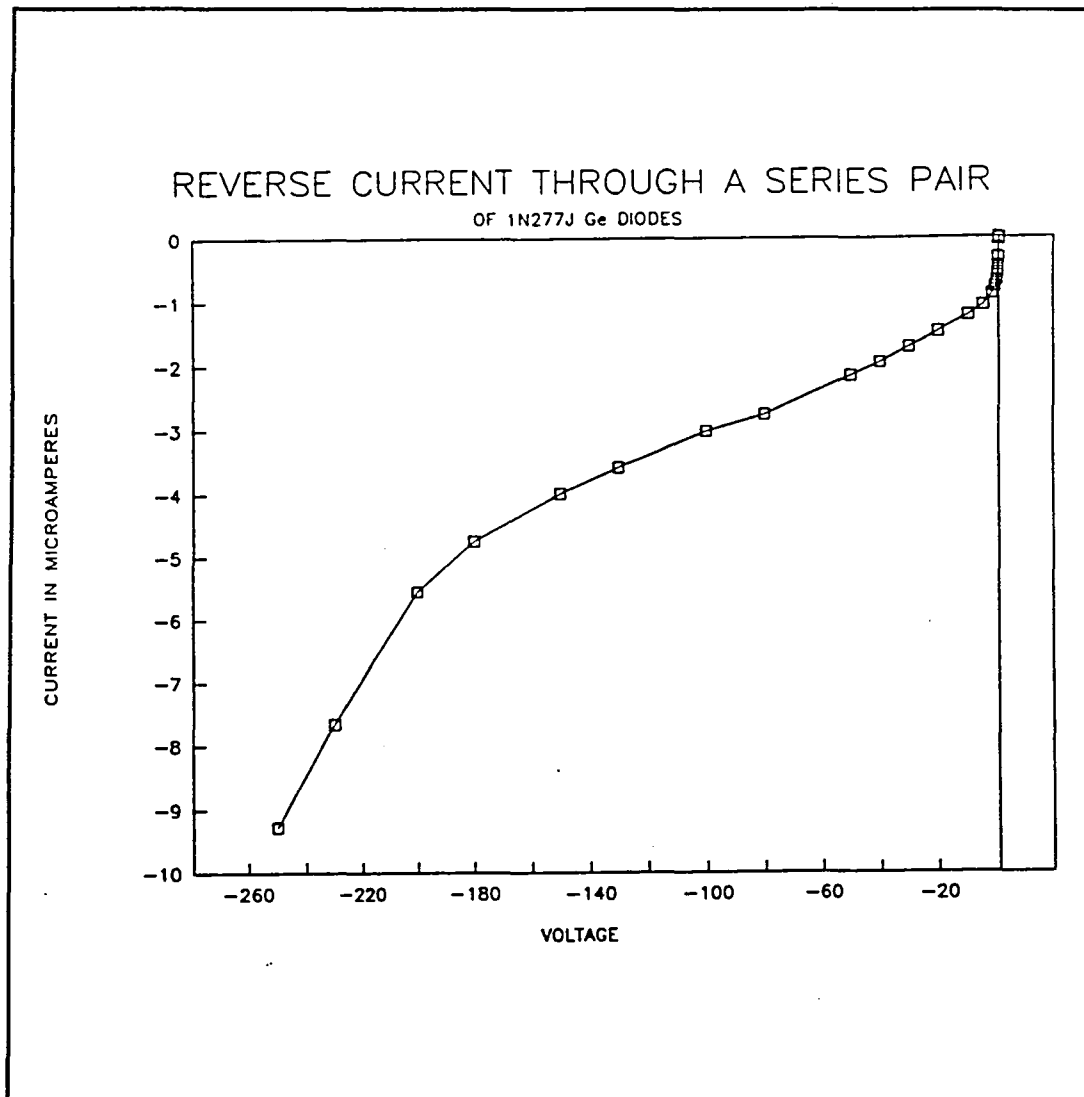


Figure 8. Current vs Voltage for a Pair of 1N277J Diodes

volume will be occupied by one limiter.

The recommendation for the choice of current limiter is the circuit shown in Figure 1. Only n-channel JFETs are needed and these are easier to obtain than p-channel JFETs with low pinch-off voltage and high breakdown voltage.

ACHIEVING TWO-FAULT TOLERANCE

Again, because little is known about how op amp input circuits fail it is not recommended that they be considered as one level of fault tolerance. What is recommended is to series three current limiters in each of the patient leads. Thus it

would take three times the breakdown voltage of an individual limiter to cause the three to breakdown. Since these are in series the current protection would be that of the individual limiters. A disadvantage of placing three limiters in series is that the total resistance is three times that of an individual limiter. Thus thermal noise voltage will have to increase to obtain two-fault tolerance.

SIGNAL CONDITIONER SPECIFICATIONS

The amplitude and frequency content of the ECG and EMG will determine some of the signal conditioner specifications. The amplitude of the ECG is .1-4 mV (Olson, 1978) and the recommended 3 dB bandwidth is .05 to 100 Hz (Kossman, 1967). Pipberger et al. (1975) also recommend that the response of any EMG amplifier be flat within $\pm .5$ dB in the range of 0.14 to 25 Hz. The amplitude of the EMG is .1-1 mV for surface electrodes. If needle electrodes are used for the EMG much larger voltages, up to 90 mV, can be recorded. The bandwidth required for the EMG is 25 to several kHz (Neuman, 1978). A maximum bandwidth of 1000 Hz is recommended since most clinical studies rarely use bandwidths in excess of 500 Hz. The amplitude out of the signal conditioners should be 5 V or less and should be designed with flexible gain. The gain is recommended to be from 400 to 8000. This would amplify a .1 mV signal to a level of .8 V and a signal of 12.5 mV will not exceed 5 V.

The input impedance of any ECG or EMG amplifier should be as large as possible. This will reduce any voltage divider effect caused by the sum of the total source impedance (skin impedance, electrode impedance, and current limiter impedance) and the input impedance of the amplifier. High input impedance will also reduce any effective input voltage caused by a common mode voltage and source impedance imbalance. The recommended input impedance is at least 5 M Ω by Pipberger et al. (1975). Hauta and Webster (1973) also recommend a 5 M Ω input impedance to keep a source impedance imbalance of 5 k Ω and a common mode voltage of 10 mV from causing more than 10 μ V if equivalent input voltage. A value of 10 μ V corresponds to 1% of a typical 1 mV input ECG signal.

The common mode rejection ratio, CMRR, of the amplifier should also be as large as possible to reduce the output voltage caused by any signal common to the inputs. Hauta and Webster (1973) recommend a modest 60 dB CMRR at 60 Hz with a 5000 Ω source impedance imbalance.

Random noise is always present in resistors and amplifier electronics. This random noise can be expressed in rms or peak-to-peak voltages. The peak-to-peak voltage is typically a factor of 6 to 8 times the rms voltage (Horowitz and Hill, 1989, p. 454). The peak noise when referred to the input should be no more than about 1% of the input signal level. This would correspond to about 2 μ V of peak-to-peak node voltage (.25-.33 μ Vrms) for the lowest expected 0.1 mV input signals.

Other specifications of the signal conditioning circuits are as follows. They should be battery powered for portability. Since they are battery powered, they should consume as little power as possible. The output resistance should be as small as possible. Since there exists the possibility of more than one signal conditioner connected to an astronaut, it is recommended that the reference electrode be connected to power supply ground

(through the current limiters) as opposed to using some type of "driven right leg" system. With multiple driven systems connected at a time the possibility exists for them to "buck" one another and have an oscillatory reference voltage on the body. The output voltage level should be ± 5 V and there should also be an output that has a 2.5 V output level for zero input signal.

SIGNAL CONDITIONER DESIGN

The choice of an op amp to be used for the input stages of the instrumentation portion of the signal conditioners was based on the power consumption of the op amp and its noise parameters. Noise is generated at the input of the amplifier due to noise from the input resistors and from the input amplifier. The noise associated with the input resistors is due to thermal noise, shot noise and flicker ($1/f$) noise. According to Horowitz and Hill (1989, pp. 430-432) for metal film or wire-wound resistors the main component is due mostly to the thermal noise, which is a "white" noise. The total noise voltage in rms is

$$E_{thermal} = 4kTR(f_H - f_L)^{\frac{1}{2}}. \quad (3)$$

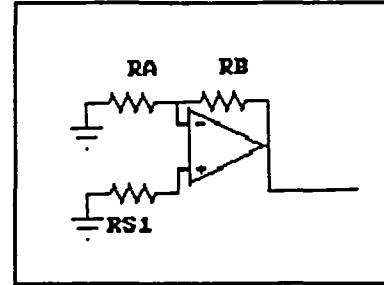


Figure 9. Single Op Amp.

The constant $4kT$ has a value of $1.6E-20$ at room temperature.

R is the resistance value, and the frequency bandwidth of interest is given by $f_H - f_L$, the upper and lower frequencies of the band.

The noise associated with the input stages of the op amp can be represented by noise current sources and a noise voltage source. The noise and current sources have noise density power spectra that are composed of flicker noise at low frequencies up to some corner frequency (which is generally different for the noise current and noise voltage sources) and a constant ("white") noise power spectrum from this corner frequency out to infinity. In Figure 9 is shown an op amp with both inputs grounded. R_{S1} is the source resistance seen by the positive terminal of the op amp and R_{S2} is the parallel combination of resistors R_A and R_B . The total noise in a given bandwidth associated with this stage is given by

$$\begin{aligned} E^2(f_H - f_L) = & e_n^2 \times \left[f_{nvc} \cdot \ln\left(\frac{f_{nvc}}{f_L}\right) + (f_H - f_{nvc}) \right] \\ & + i_n^2 \times \left[f_{nvc} \cdot \ln\left(\frac{f_{nvc}}{f_L}\right) + (f_H - f_{nvc}) \right] \times (R_{S1}^2 + R_{S2}^2) \\ & + 4KT(f_H - f_L)(R_{S1} + R_{S2}). \end{aligned} \quad (4)$$

The white noise voltage, in $V/\sqrt{\text{Hz}}$, is given by e_n and the white noise current, in $A/\sqrt{\text{Hz}}$,

is given by i_n . The corner frequencies of the current and voltage are f_{nc} and f_{nv} respectively. Equation 4 is for the case when f_{nc} and f_{nv} are between f_L and f_H . If the corner frequencies are less than f_L then their respective bracketed term will change to

$$[f_H - f_L] . \quad (5)$$

If the corner frequencies are greater than f_H , then their respective bracketed terms will be given by

$$[f_{nc} \ln(f_H/f_L)] . \quad (6)$$

The first term in the Equation 4 is due to the amplifier equivalent noise voltage source. The second term is the voltage due to the amplifier equivalent noise current sources flowing through R_{S1} and R_{S2} . The log term in each of these expressions is due to flicker noise. The last term in the expression is the thermal noise of R_{S1} and R_{S2} . Because of the random nature of these noises, the noise powers (and not noise voltages) add. The development of

Equation 4 can be found in Meiksin and Thackray (1984, p. 131). The errors in the formula as presented by Meiksin and Thackray have been corrected here.

The input stage of the signal conditioners will be the standard three op amp differential amplifier. The first two op amps of such a design are shown in Figure 10. The total noise referred to the input will then be due to each of these. Since the noise powers add, the total noise will be given by

$$E_{total} = \sqrt{E_+^2 + E_-^2} \quad (7)$$

E_+ and E_- will be the noise voltage associated with the op amp of the + and - terminals of the overall instrumentation amplifier. Each of their voltages is given by Equation 4. R_{S2} for each op amp is simply the feedback resistor since all the bias currents for their negative inputs passes through those resistors.

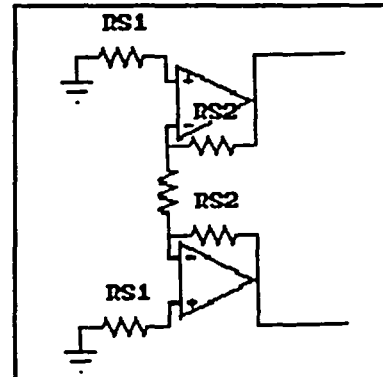


Figure 10. Two Op Amp Input Stage.

Micropower Operational Amplifiers

In this investigation several micropower op amps were examined for their noise characteristics. A list of those op amps considered is given in Table 1 along with the noise parameters of these op amps. Table 2 shows the total noise voltage associated with the two front end op amps for the two different bandwidths of interest, i.e., .05-100 Hz for the ECG signal conditioner and 25-1000 Hz for the EMG signal conditioner. Also shown in this table are several parameters of interest for the op amps: the quiescent power supply current, the bias current, the gain bandwidth product (GBP), and the slew rate. The noise numbers were generated with R_{S1} and R_{S2} equal to

100 and 200 k Ω respectively. R_{S1} was chosen to represent a combination of skin resistance, electrode resistance, and current limiter resistance.

TABLE 1. MICROPOWER OP AMPS AND THEIR NOISE PARAMETERS

op amp	type	E_n V/ $\sqrt{\text{Hz}}$	F_{nvc} Hz	I_n A/ $\sqrt{\text{Hz}}$	F_{nic} Hz
LT1078	BJT	2.8e-08	7.0e-01	1.7e-14	1.5e+02
LT1178	BJT	4.9e-08	*5.0e-01	1.0e-14	*4.0e+01
LM146	BJT	8.5e-08	1.0e+00	1.8e-13	1.0e+01
LF441	JFET	3.3e-08	2.0e+01	1.0e-14	1.0e+02
OP20-B	BJT	8.0e-08	2.0e+00	9.0e-14	2.0e+01
OP22(1UA)	BJT	9.0e-08	4.0e+00	1.8e-13	2.0e+00
OP22(10UA)	BJT	3.7e-08	6.0e+00	3.7e-13	6.0e+00
OP220	BJT	4.0e-08	3.5e+00	9.0e-14	1.5e+01
OP90	BJT	6.0e-08	8.0e+00	7.0e-13	9.0e+01
TLC27L2	CMOS	7.0e-08	1.0e+01	0.0	1.0e+00
TLC1078	CMOS	7.0e-08	9.0e+00	0.0	1.0e+00

* Personnel communication with an application engineer.

TABLE 2. NOISE VOLTAGE AND OTHER PARAMETERS FOR SELECTED MICROPOWER OP AMPS.

op amp	type	R1 ohm	R2 ohm	E_{total} .05-100 Hz 2 OP AMPS μVrms	E_{total} 25-1000 Hz 2 OP AMPS μVrms	Quiescent supply current μA	Bias Current nA	GBP kHz	Slew Rate V/usec
LT1078	BJT	1E+05	2E+05	1.07	3.30	39.0	7.0	200.0	0.070
LT1178	BJT	1E+05	2E+05	1.20	3.75	14.0	6.0	60.0	0.025
LM146	BJT	1E+05	2E+05	1.70	5.16	35.0	20.0	100.0	0.040
LF441	JFET	1E+05	2E+05	1.18	3.39	150.0	0.1	1000.0	1.000
OP20-B	BJT	1E+05	2E+05	1.57	4.76	55.0	25.0	100.0	0.050
OP22(1UA)	BJT	1E+05	2E+05	1.77	5.32	160.0	35.0	250.0	0.080
OP22(10UA)	BJT	1E+05	2E+05	1.73	5.04	16.0	7.5	15.0	0.008
OP220	BJT	1E+05	2E+05	1.21	3.64	70.0	20.0	200.0	0.050
OP90	BJT	1E+05	2E+05	5.95	8.16	14.0	20.0	25.0	0.012
TLC27L2	CMOS	1E+05	2E+05	1.54	4.35	14.5	0.6	110.0	0.050
TLC1078	CMOS	1E+05	2E+05	1.52	4.35	14.5	0.6	110.0	0.047

From Table 2 the candidates for the op amps to be used are either the LT1078 or the LT1178 since these have the lowest total noise and the smallest quiescent power supply current. It should be noted that these predicted noise voltages are higher than the recommended values of .25-.33 μV . However, those values were based on an input signal amplitude of only .1 mV. The typical input signal is generally about 1 mV. For this

level of signal, the random noise would be less than 1% of the input signal.

The predicted noise voltages for these two op amps were experimentally verified using fixed resistors. The noise generated using electrodes was actually higher by a factor of four than the predicted values. This is probably due to random fluctuations of the electrode half-cell potential; a factor not accounted for in the noise model.

The choice between the LT1078 and the LT1178 can be made based on the other parameters listed in the table. The slew rate needed for the op amp is determined by the last op amp of the design and is given by

$$\text{slewrate} = 2\pi f_{\max} V_{\text{out}} \quad (8)$$

$$2\pi (1000\text{Hz}) 5\text{V} = .314\text{V}/\mu\text{sec}.$$

The maximum frequency required is for the EMG signal conditioner and is 1000 Hz. The maximum output voltage required is 5 V. Given this value of slew rate, only the LT1078 will be satisfactory. This op amp is very attractive for purposes of the signal conditioner because the power supply current is only 39 μA . It is also available in die form.

Figure 11 shows the first stage of the signal conditioner. This stage is the standard three op amp differential amplifier. The overall gain of this stage is 400 (the minimum for the signal conditioners). The gain is split evenly between the first section and second section, i.e., 20 for each. With a GBP of 200 k this will allow each stage to pass frequencies up to 10 kHz. The CMRR of the first stage is 26 dB (common gain of 1 and a difference gain of 20). The worst CMRR of the second section using .1% resistors is 74 dB. The CMRR of the second stage op amp sets the limit for the stage. The CMRR of the LT1078 is 106 dB which is much higher than 74 dB predicted for the second stage. Thus, the limit on CMRR of the second stage will come from the resistors used. The resistors used in the first section should be metal film or wire wound to reduce shot and flicker noise in these resistors.

It is desirable to alter the value of one of the resistor values specified in this design. If the 200 k Ω feedback resistors are changed to 20 k Ω the total random noise, referred to the input, drops from 1.07 μVrms to .74 μVrms .

Figure 12 shows the filtering sections. The output of the first stage will go to a first-order high-pass filter. The 3 dB frequency is given by $1/(2\pi RC)$. For the values shown, the break frequency is approximately .05 Hz. The break frequency can be changed to approximately 25 Hz for the EMG signal conditioner by changing the resistor value to 13.7 k Ω . Also shown in this figure is a fourth-order voltage controlled voltage source, VCVS, Butterworth low-pass filter. This filter provides maximum flatness in the pass-band and very good attenuation in the stop-band. For this filter

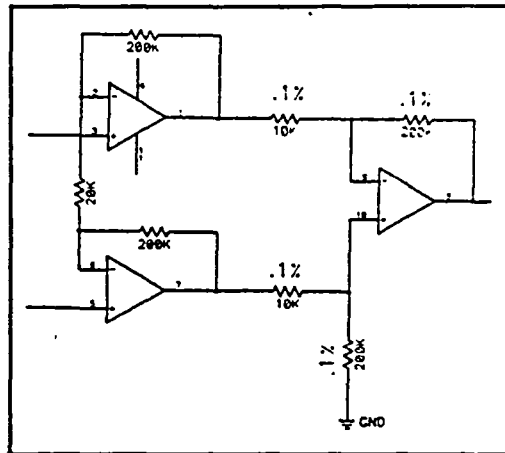


Figure 11. First Stage of the Signal Conditioner.

$R_{11}=R_{12}=R_{21}=R_{22}=R$ and $C_{11}=C_{12}=C_{21}=C_{22}=C$. The 3 dB frequency is given by $1/(2\pi RC)$. If $R = 158 \text{ k}\Omega$ and $C = .01 \mu\text{F}$, then the 3 dB frequency will be approximately 100 Hz. One percent component values should be used since SPICE analysis showed that for the worst case the magnitude response is only off by 0.5 dB. For two percent values the magnitude response can be off by 1.2 dB in magnitude for the worst case. R_{14} should be equal to $.152R_{13}$ and R_{24} should be equal to $1.235R_{23}$. For a 3 dB frequency of 1000 Hz. then $R_{11}=R_{12}=R_{21}=R_{22}= 15.8 \text{ k}\Omega$. The gain of the filter section is 2.575.

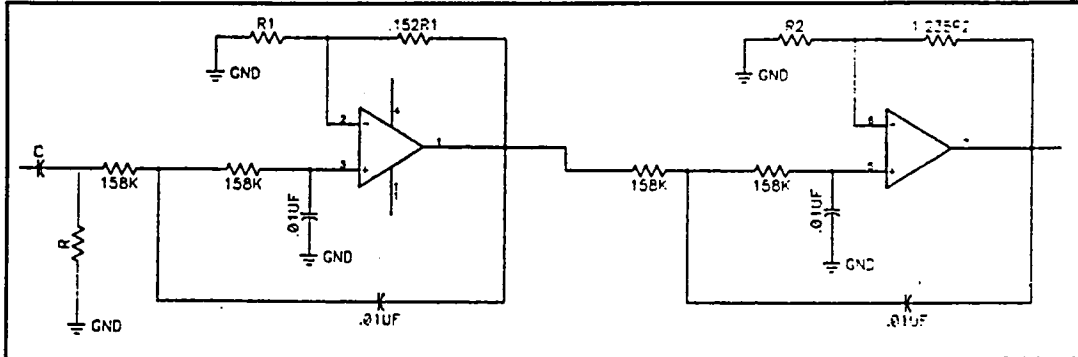


Figure 12. Filter Section of the Signal Conditioner.

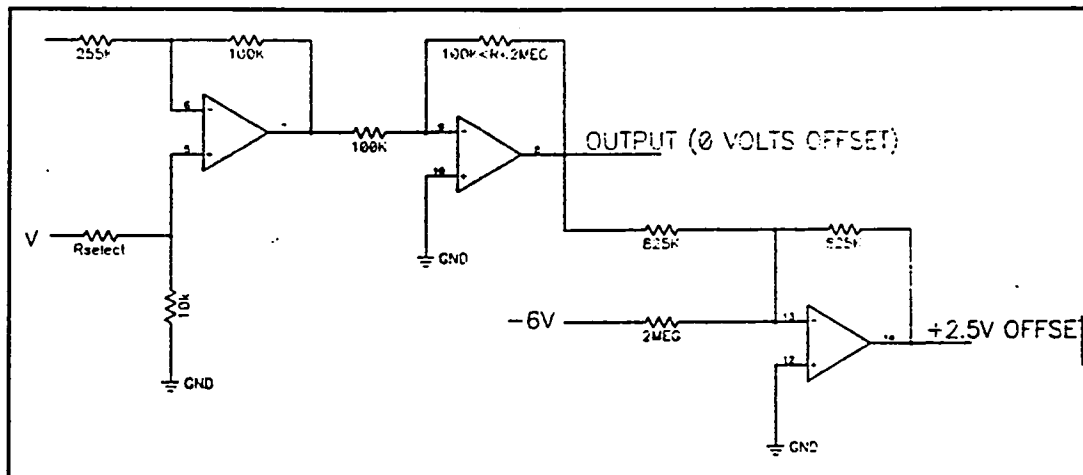


Figure 13. Last Stage of the Signal Conditioner.

The final stage of the signal condition is shown in Figure 13. The signal from the filter section is applied to the 255 k Ω resistor. The gain of this noninverting amplifier is 1/2.55 to negate the gain of the filter section. The V applied to R_{select} is either plus or minus 6 V, the power supplies voltages, and the value of R_{select} is chosen to remove offset voltages of the amplifier. The next stage is a noninverting amplifier that has a gain from 1 to 40, yielding an overall gain of 400 to 8000. The value of the feedback resistor, R, is chosen to yield the desired gain. (Using the LT1078, this op amp could have a gain of 200 and still not limit the bandwidth of the EMG signal.) The output is taken from this

op amp if zero offset voltage is desired. The last op amp simply provides for a +2.5 V offset voltage to the output signal for the ECG signal, if it is desired.

To provide for maximum flexibility only a few resistors need to be changed to make the basic design adaptable to the ECG or EMG signal conditioner. These resistors, R_{11} , R_{12} , R_{21} , R_{22} , R_{select} , and R can be normal resistors that are not in the hybrid circuit by are soldered in a dip header.

The input resistance of the LT1078 is typically 800 M Ω differentially and 6 G Ω common mode. The actual differential input resistance will be higher than 800 M Ω . It will be this value increase by the loop-gain of the first stage. In reality surface effects on the hybrid circuit will cause this resistance to be lower than this very high value. However, it will still be much larger than the recommended value of 5 M Ω .

The output impedance of the LT1078 is 10 Ω for the gain and frequencies of this design. This is well below the recommended value of 200 for the EMG amplifier.

The output voltage of the LT1078 op amps will go down to the minus supply and will go up to 1 V less than the positive supply voltage. Therefore plus and minus 6 V supplies will provide the required 5 V output swing. Batteries made from a series connection of 1.5 V button silver oxide batteries each with 38 mAh life would work well for the supplies. Since there are eight op amps in the design each pulling 39 μ A from each supply, the life of the signal conditioners should be $38 \text{ mAh} / (8 * 39 \text{ } \mu\text{A}) = 122$ hours.

SUMMARY

Modification of the signal conditioning circuits for the EMG and the ECG was investigated in this study. It is recommended that two-fault tolerance be achieved with the JFET current limiters shown in Figure 1. Three of these devices should be placed in series with each of the electrode leads. It is also recommended that the new signal conditioner amplifiers be based on the LT1078 op amp due to its relatively low noise voltage in comparison to other micropower op amps.

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